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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,753	03/22/2005	Philippe Maugars	FR02 0101 US	4743

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
10/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/528,753	MAUGARS, PHILIPPE	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/528753 Attorney's Docket #: FR020101US
Filing Date: 3/22/05; claimed foreign priority to 9/25/02

Applicant: Maugars

Examiner: Alexander Williams

Applicant's Amendment filed 10/12/2006 has been acknowledged.

Claim 4 has been cancelled.

Claims 1-3 and 5 to 11 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by "contact pins emerging above said upper surface to contact **a chip card**, contact pins emerging below said lower surface to contact a board, **a circuit** comprising contact tabs." Is the chip card the same as a circuit? Otherwise, where is both elements shown in the drawings? Please explain.

In claim 2, it is unclear and confusing to what is meant by "contact pins emerging above said upper surface to contact **a chip card**, contact pins emerging below said lower surface to contact a board, **a circuit** comprising contact tabs. Is the chip card the same as a circuit? Otherwise, where is both elements shown in the drawings? Please explain.

Any of claims 1-3 and 5 to 11 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on contact pins, holding means and contact tabs deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1-3, 5 and 7 to 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killcommons (U.S. Patent # 4,907,976).

1. Killcommons (figures 1 to 10) specifically figure 7 show a connector comprising: an upper surface **(shown in figure 7 on the bottom side)** and a lower surface **(top of 46)**, contact pins **14** emerging above said upper surface to contact a chip card **10**, contact pins **32** emerging below said lower surface to contact a board **(discuss but not shown)**, and a cavity **(area in which 12,10 sits)** in said upper surface to receive a circuit **10** comprising contact tabs **32**, said cavity comprising contact surfaces **(sides of 46)** connected to said contact pins to contact said contact tabs and holding means **32** for holding the circuit in the cavity.
2. Killcommons (figures 1 to 10) specifically figure 7 show a connector **46** comprising: an upper surface **(shown in figure 7 on the bottom side)** and a lower surface **(top of 46)**, contact pins **14** emerging above said upper surface to contact a chip card **10**, contact pins **3** emerging below said lower surface to contact a board **20**, a circuit **1** comprising contact tabs **8**, and a cavity **(area in which 10,12 sits)** in said upper surface intended to receive said circuit, said cavity comprising contact surfaces **6** connected to said contact pins and to contact said contact tabs.
3. Connector as claimed in claim 1, Killcommons show where the cavity is placed in a central area bounded by the contact pins.
5. Connector as claimed in claim 1, Killcommons comprises additional connection means **32** for electrically connecting the contact tabs and said contact surfaces.
7. Killcommons show a Chip card reader comprising a connector as claimed in claim 1.
8. Killcommons show a Mobile telephone comprising a connector as claimed in claim 1.
9. Killcommons show a Personal digital assistant comprising a connector as claimed in claim 1.
10 and 11. The connector of claim 1 and claim 2, Killcommons show wherein at least one of the contact pins emerging below said lower surface is electrically coupled to one of the contact surfaces to electrically connect said circuit with said board, and wherein at least one of the contact pins emerging above said upper surface is electrically coupled to another one of the contact surfaces to electrically connect said circuit with said chip card.

Therefore, it would have been obvious to one of ordinary skill in the art to use the contact pins and the contact tabs

as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Killcommons (U.S. Patent # 4,907,976) in view of Panella et al. (U.S. Patent # 6,853,559 B2).

Killcommons show the features of the claimed invention as detailed above, but fail to explicitly show where the circuit comprises decoupling capacitors connected between a ground (inherent) and the contact tabs.

Panella et al. (figures 1 to 58) specifically figure 23 show a connector **112** comprising: an upper surface **(shown in figure 23 top of 112)** and a lower surface **(bottom of 112)**, contact pins **228,24,116,242** emerging about said upper surface and intended to be in contact with a chip card **114**, contact pins **220,132** emerging below said lower surface and intended to be in contact with a board **114**, a cavity **(area in which 70,58 sits)** in said upper surface intended to receive a circuit **58** comprising contact tabs **(top of 1,232)**, s where the circuit comprises decoupling capacitors **42** connected between a ground (inherent) and the contact tabs for the purpose of providing an approach bypasses the motherboard and the interposer socket, the path of current flow is shorter improves the impedence and the resulting voltage drop of the relatively shorter path.

6. Connector as claimed in claim 2, the combination with Panella et al. show where the circuit comprises decoupling capacitors **42** connected between a ground (inherent) and the contact tabs (see figures 15-19 and 26-28).

Therefore, it would be obvious to one of ordinary skill in the art to use Panella et al.'s decoupling capacitors to modify Killcommons connector for the purpose of providing an approach bypasses the motherboard and the interposer socket, the path of current flow is shorter improves the impedence and the resulting voltage drop of the relatively shorter path.

(8) Power delivery concerns supplying power to devices that need it. Traditionally, an ideal power supply is assumed and little consideration is given to power delivery until the end of the design. Printed circuit board (PCB) designers attempt to create the ideal power delivery supply with conventional power and ground planes in the PCB and with wide, heavy traces on the PCB to distribute the power among the devices on the PCB. High frequency ceramic capacitors control high frequency noise, created by switching the transistors on and off, by shorting the high frequency noise to ground. Lower frequency bulk capacitors (such as tantalum capacitors) subsequently recharged the high frequency ceramic capacitors. Various rules of thumb exist for determining the amount of each type of capacitance that is required for various ICs.

(9) To electrically model this power delivery system, considerations include the inductance and resistance of cables, connectors, PCB, pins, contacts and components, such as resistors and capacitors, of the receiving device(s) and power source(s). In the past, voltage drops due to inductance (V=L di/dt) and resistance (V=IR) have been nearly negligible relative to the tolerance of devices in most systems. Similarly, simple rules of thumb determine the method for decoupling the high frequency noise.

(18) Attempts have been made to manage surge currents by placing decoupling capacitors throughout the power delivery system such as on the voltage regulation module, the motherboard, the interposer PCB, the die package, and on the die itself. Decoupling capacitors are typically located on the circuit board outside the microprocessor package, typically using several discrete decoupling capacitors mounted next to the microprocessor package on the circuit board. In this approach, conductive traces on the circuit board connect the decoupling capacitors to power and ground pins on the microprocessor. In another approach, a discrete decoupling capacitor is formed as part of the IC.

(19) These decoupling capacitors are commonly used to ensure that the power supply system can provide the microprocessor with a surge current when required. The decoupling capacitors connect power sources to the power leads of the microprocessor. The amount of decoupling capacitance needed depends on the power requirement of the microprocessor. The microprocessor is able to draw its required surge current from the power stored in the

decoupling capacitors, and hence, the decoupling capacitors stabilize the power delivery system by storing power local to the microprocessor in order to meet the surge current needs of the microprocessor. However, use of discrete, broad-mounted decoupling capacitors not only increase the cost of the power delivery system, but also consume additional area on the IC or the circuit board, or elsewhere.

(20) As the power requirement of microprocessor increases, the need for more decoupling capacitance increases, which in turn requires larger value or size decoupling capacitors and more space to accommodate them. Unfortunately, larger value or size decoupling capacitors consume more area on the circuit board.

(21) As the switching speeds of the transistors increases, an undesirable amount of resistance due to inductance, associated with the interconnection between the semiconductor die and the decoupling capacitor, increases according to the formula (X.sub.L =2[character pullout]fL). The longer the conductive path interconnecting the decoupling capacitor and the semiconductor die inside the microprocessor, the higher the inductance. The higher the frequency of operation of the microprocessor, the higher the resistance of the system due to the inductance, and higher resistance causes a higher voltage drop. Therefore, it is desirable to locate the decoupling capacitors as close to the semiconductor die as possible, such as by putting the decoupling capacitor inside the microprocessor package, as described above, in order to minimize the conductive path to minimize the inductance.

(22) Further, capacitors exhibit inductance and resistance characteristics as well as capacitance characteristics and can be electrically modeled as a series RLC circuit. At higher frequencies, such as above 100 MHz, the inductance characteristic limits the effectiveness of conventional discrete decoupling capacitors. If large surge currents are required by the microprocessor, this residual inductance can cause unacceptable voltage drops and AC noise.

FIGS. 24 to 26 illustrate package design systems 16 for the IC 22 having power contacts located on the top of the IC 22. FIG. 27 illustrates an assembly of the system 10 using the IC 22, as shown in FIG. 26. FIGS. 28 to 31 illustrate various assembly views of the system 10. FIGS. 32 and 33 illustrate the connector 112, formed as a socket or a cover, having the

decoupling capacitance 42, formed as an integral capacitor. FIGS. 34 to 44 illustrate various embodiments of the decoupling capacitance 42, formed as an integral capacitor, carried by a separate or integral connector 112, formed as a cover, a socket or a frame. FIGS. 45 to 60 illustrate various embodiments of the decoupling capacitance 42, formed as multiple discrete capacitors, carried by the connector 112, formed as a cover, a socket or a frame.

Response

Applicant's arguments filed 8/2/07 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/690-690,696,698,666,668,678,723,724,730,704,735, e23.178,e25.012,e23.061,e23.079,e23.004,e23.062,e23/0 36,e23/052,e23.178,e23.172,e23.061 439/76.1,50,66,34,736 361/764,704,785,803,760,762,767,795,729 174/52.4,262 29/883,854,855,856	7/7/06 1/28/07 10/14/07
Other Documentation: foreign patents and literature in 257/690-690,696,698,666, 668,678,723,724,730,704,735,e23.178,e25.012,e23.061,e 23.079,e23.004,e23.062,e23/036,e23/052,e23.178,e23.17 2,e23.061 439/76.1,50,66,34,736 361/764,704,785,803,760,762,767,795,729 174/52.4,262 29/883,854,855,856	7/7/06 1/28/07 10/14/07
Electronic data base(s): U.S. Patents EAST	7/6/06 1/28/07 10/14/07

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
10/14/07